REMARKS

Entry of the foregoing amendments after final rejection as narrowing the issues and presenting the claims in condition for allowance or better form for appeal is solicited. The foregoing amendments after final rejection have not been earlier presented because of the new grounds for rejection.

Claims 1, 3, and 5-9 are at issue. Claims 1, 3 and 5-9 were rejected as unpatentable over Yilmaz et al. (U.S. Pat. 5,751,054) in view of Imoto (U.S. Pat. 5,920,781). The applicant respectfully traverses the rejections. Reconsideration is requested.

The applicant submits that claim 1 is not obvious over Yilmaz et al. in view of Imoto. The action does not make out a *prima facie* case of obviousness. Neither Yilmaz et al. nor Imoto teaches or suggests all of the limitations of independent claim 1. In particular, claim 1 recites that a slanted side wall of the gate electrode of the DMOS element overlaps a source region and another slanted side wall does not overlap a drain region. Although Yilmaz et al. disclose a DMOS transistor having a gate electrode (110A), Yilmaz et al. also disclose that the gate electrode (110A) does not overlap the source region (152) (Figs. 15A, 16A). In other words, Yilmaz et al. do not disclose a portion of the gate electrode overlapping a part of the source region. Further, Yilmaz et al. do not disclose that the DMOS transistor includes a gate electrode having slanted side walls, as noted in the action (07/13/2004 action, p. 4). As such, Yilmaz et al. do not disclose a portion of a slanted side wall of a gate electrode overlapping a part of a source region, as recited in claim 1.

Imoto does not disclose a portion of another slanted side wall not overlapping the drain region (col. 3, ll. 35-40). In particular, Imoto discloses only source regions (19, 20). Imoto does not disclose drain regions. As such, Imoto does not disclose a side wall that does not overlap a drain region, as recited in claim 1.

Further, claim 1 recites that the gate electrodes of the DMOS element and the MOS element have different side wall profiles. Although Yilmaz et al. disclose a DMOS transistor and an NMOS transistor formed on a substrate, Yilmaz et al. do not disclose that the transistors include gate electrodes having different side walls profiles. Instead, Yilmaz et al. teach a DMOS transistor and an NMOS transistor having gate electrodes (110A, 110E) with square side wall profiles (Fig. 16A). The side wall profiles for each of the gate electrodes is the same. Further, as

noted in the action (7/13/2004 action, p. 4), Yilmaz et al. do not disclose that the DMOS transistor includes a gate electrode having slanted side walls. Instead, each of the gate electrodes of Yilmaz et al. have side wall profiles that are square. Yilmaz et al. therefore does not disclose a MOS element including a gate electrode having side walls with a different profile than the slanted side walls of a gate electrode of a DMOS, as recited by claim 1.

Likewise, although Imoto discloses that a polysilicon gate electrode (13) of an N-channel MOS transistor may include tapered side parts (15, 16) (col. 2, ll. 57-64), Imoto does not disclose a MOS element formed on the same substrate as a DMOS element, much less a gate electrode for the MOS element. As such, contrary to the action, it is impossible for Imoto to disclose a MOS element having a gate electrode having side walls with a different profile than slanted side walls of a DMOS element, because Imoto discloses only one gate electrode. There is no other gate electrode with a side wall profile available for comparison. Therefore, Imoto does not disclose a MOS element including a gate electrode having side walls with a different profile than the slanted side walls of a gate electrode of a DMOS. The action's rejections of claim 1 and claims 3 and 5-9 dependent thereon are therefore improper for failing to cite references that teach or suggest all of the claims limitations of independent claim 1, whether taken individually or in combination. It is clear that a *prima facie* case of obviousness cannot be established where all the limitations of a claimed combination are not taught or suggested by the prior art. See *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). See also MPEP 2143.03.

It is further submitted that the action does not establish a *prima facie* case of obviousness because Imoto teaches away from the combination of Yilmaz et al. in view of Imoto. In particular, Imoto teaches away from the gate electrodes of Yilmaz et al. Yilmaz et al. discloses gate electrodes having square side wall profiles. Imoto discloses that square side wall profiles, as used in Yilmaz et al., result in: 1) smaller impurity concentrations which cause a punch-through phenomenon and adversely affect the voltage-resistance of the transistor; or 2) a drive-in process at a higher temperatures and for a longer period of time which adversely affects the general characteristics of the transistor element (col. 1, ll. 37-61; Figs. 6A-6D). Imoto thereby expressly teaches away from a gate electrode having side walls with a square profile, as disclosed by Yilmaz et al. One of ordinary skill in the art would therefore not be motivated to provide a gate electrode as disclosed by Imoto and a gate electrode as disclosed by Yilmaz et al. in the same circuit because Imoto teaches away from the gate electrode of Yilmaz et al.

Therefore, Imoto and Yilmaz et al. cannot be properly combined to disclose a gate electrode having slanted side walls with a different profile than the slanted side wall of another gate electrode, as recited in claim 1.

The rejections of claim 1 and claims 3 and 5-9 dependent thereon are therefore improper because the references teach away from each other, and cannot be combined. A *prima facie* case of obviousness cannot be established where the references teach away from their combination. See MPEP 2145(X)(D)(2).

Accordingly, the applicant respectfully submits that all pending claims are patentable over the art of record and should be allowed. In light of the foregoing, the prompt issuance of a notice of allowance is respectfully solicited.

Should the examiner have any questions, the examiner is respectfully invited to telephone the undersigned.

Respectfully submitted,

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